USN [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]   **12EC121**

M.Tech. Degree Examination, June/July 2014
Digital System Design using Verilog

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1   a. What is meant by the term design methodology? Why is it beneficial? With a neat flow chart explain design methodology for hardware/software co-design. **(10 Marks)**

    b. Develop a sequential circuit with a single data input S and a single data output Y. The output is 1 when the input value in the current clock cycle is different from the input value in the previous clock cycle. Write the verilog code using structural modeling method to realize the circuit. **(06 Marks)**

    c. Design a digital circuit for a night-light that is lit when the switch is ON and to select between activating the light when it is dark and activating the light during night-time hours. Assume there is a timer that produces a 1 output at night. **(04 Marks)**

2   a. One hot code is used for state of a road traffic light. The possible states behind red, yellow and green. Develop a verilog model for the light controller that has encoded input, x encoded output, and single-bit input that enables the lights. When enable is 1, encoded output is same as encoded input else all outputs are 0. Develop a test bench model for the light controller module. **(12 Marks)**

    b. Use a 2 to 1 multiplexer to implement a circuit whose output is given by the Boolean expression $a \cdot (b + \bar{c})$ when enable set is 1, and by Boolean expression $x \oplus y$ otherwise, develop the verilog model. **(05 Marks)**

    c. Draw a schematic for a buffer tree to drive 12 inputs from a source, assuming that the source and each buffer can each drive at most three inputs. **(03 Marks)**

3   a. Discuss the operations performed on signed integers with relevant illustrations and expressions. **(10 Marks)**

    b. With relevant equations discuss about fast carry chain full adders. Draw the two fast adders and explain their working. **(07 Marks)**

    c. What is the range and precision of each of the following unsigned fixed-point representations with m pre-binary point and f post-binary point bits?
    i)   12 bits, with m = 5, f = 7
    ii) 10 bits, with m = -2, f = 12
    iii) 8 bits, with m = 12, f = -4. **(03 Marks)**

4   a. Develop a data path to perform complex multiplication of two complex numbers. The operands and product are in Cartesian form. The real and imaginary parts of the operands are represented as signed fixed point numbers with 4 pre-binary point and 12 post-binary point bits. The product has 8 pre-binary and 24 post-binary point bits. The complex multiplier has two fixed point multiplier components. Design the control sequence for the control signals of the sequential complex multiplier. Develop a finite state machine to implement the control sequence. Show transition and output functions both in tabular form and in state transition diagram. **(15 Marks)**

    b. Explain Register-to-Register path and timing. **(05 Marks)**

5 a. Design a circuit that computes the function $y = C_i \times x^2$, where x is a binary-coded input value and C_i is a coefficient stored in a flow-through SSRAM. X, C_i and y are all signed fixed-point values with 8 pre-binary point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start is 1. The circuit should minimize area by using a single multiplier to multiplier ci by x and then by x again. Explain with timing diagram. **(08 Marks)**

b. Using the hamming code, determine whether there is an error in the following ECC words. If so, determine the corrected ECC word and original data value:
i) 100100011010　　　　ii) 000110111000 **(06 Marks)**

c. Draw a schematic diagram showing connection of components to form $1M \times 8$ bit memory. **(06 Marks)**

6 a. List the Gumnut instruction set and their description. **(11 Marks)**

b. Show the connection between an 8051 microcontroller and separate instruction and data memories. The size of instruction memory is $64K \times 8$-bit ROM and size of data memory is $64K \times 8$ bit asynchronous SRAM. ROM has same control signals as SRAM except for the $\overline{WE}$ signal. **(07 Marks)**

c. What Gumnut instruction are encoded by the following 18-bit hexadecimal values?
i) 009C0　　　　ii) 3353D **(02 Marks)**

7 a. Discuss about the architecture for sobel accelerator data path. **(10 Marks)**

b. Design an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. Develop a verilog model of the controller. **(10 Marks)**

8　Write short notes on:
a. Synthesis
b. Area optimization
c. Timing optimization
d. Design optimization **(20 Marks)**

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